StreamDSP LLC
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IP Datasheet

Serial FPDP

for Altera and Xilinx FPGAs

Serial Front Panel Data Port is an industry standard, low-overhead, low-latency, high speed serial communications protocol. sFPDP is ideal for use in applications such as high-speed communication system backplanes, high-bandwidth remote sensor systems, signal processing, data recording, and high-bandwidth video systems. The simple and lightweight nature of the protocol makes it an attractive choice for replacement of parallel bus interconnects using serial transceiver technology. sFPDP can be used in point-to-point or loop topologies, uni-directional or bi-directional links, and easily supports different types of data with efficient and flexible data framing options.

StreamDSP is committed to performance, efficiency, and flexibility. Our sFPDP core is unique in that we support nearly all transceiver based devices from Altera and Xilinx. We're always making improvements to the core with innovative new features such as multi-lane bonding for increased bandwidth, and we're continually updating the core to support new transceiver based devices offered by both Altera and Xilinx. Our core provides a open interface to the FPGA transceiver, giving the user complete control over transceiver speed, settings and adjustments. A complete reference design is provided for each family, as well as a thorough testbench with support for Aldec's Active-HDL and Riviera-Pro as well as Mentor's ModelSim tools. In addition, our testing procedure includes exhaustive Altera <-> Xilinx interoperability testing to ensure compatibility.

StreamDSP is committed to delivering the highest level of customer support to ensure a smooth system integration. We also offer IP core customization and FPGA design services.

Features

- ☑ VITA 17.1-2003 Compliant
- ☑ Conforms to FC-PH disparity rules
- ☑ Multi-lane channel bonding wrapper
- ☑ Independent data / system clock domains
- ☑ 600 Mbps to 10+ Gbps serial rate support
- ☑ Optional flow control and CRC
- ☑ 32-bit user data interface
- ☑ Basic control/status interface
- ☑ Unidirectional and bidirectional support
- ☑ Optional link startup "junk filtering"
- ☑ All sFPDP frame types supported
- Unframed data
- Single frame data
- Fixed size repeating frame data
- Dynamic size repeating frame data
  - ☑ All sFPDP system configurations
    - Basic System
    - Flow Control
    - Bidirectional Data Flow
    - Copy Mode
    - Copy/Loop Mode

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Details

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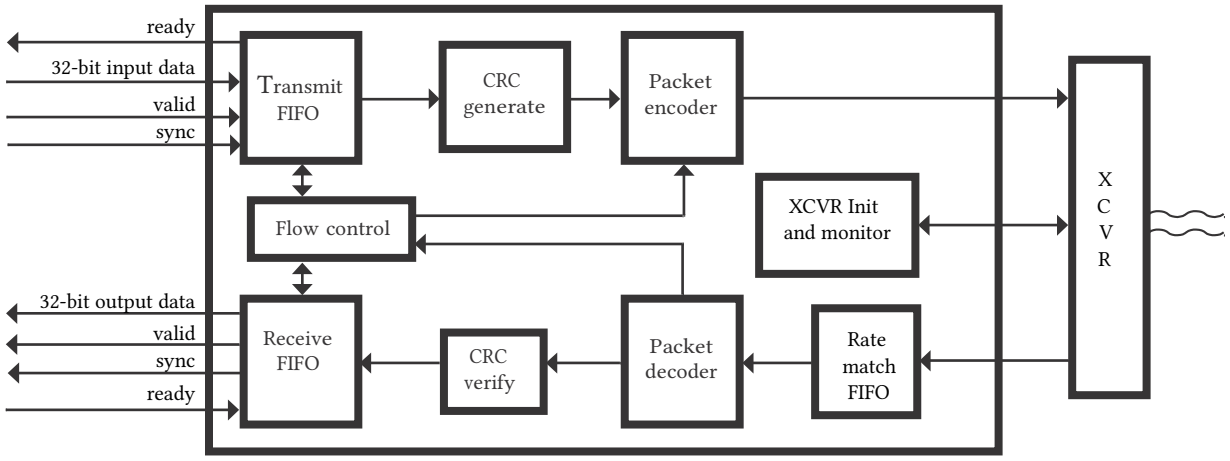

Resource Usage

Registers	LUTs	*RAM
772	841	14 Blocks

* RAM size dependent on user controlled TX and RX FIFO depths

Throughput (per lane)

Line Rate	Throughput
2.5 Gbps	247 MB/s
4.25 Gbps	420 MB/s
5.0 Gbps	494 MB/s
6.375 Gbps	630 MB/s
8.5 Gbps	841 MB/s
10.0 Gbps	990 MB/s

Delivery Options

HDL Language: **VHDL**
License Types:
- Netlist
- Source Code

* Free, supported evaluations available on request

FPGA Family Support

	Example Design
ALTERA	
• Cyclone-IV GX	Altera Cyclone-IV GX Starter Kit
• Cyclone-V GX/SX	Arrow Cyclone-V SoCkit
• Arria GX	Altera Arria-GX PCIe Dev Kit
• Arria-II GX	Altera Arria-II GX PCIe Dev Kit
• Arria-V GX	Altera Arria-V GX Starter Kit
• Arria-10 GX	BETA (Full working TB and example)
• Stratix-II GX	Altera Stratix-II GX PCIe Dev Kit
• Stratix-IV GX	Altera Stratix-IV GX PCIe Dev Kit
• Stratix-V GX	Altera Stratix-V GX PCIe Dev Kit
XILINX	
• Virtex-2 Pro	Custom Hardware board
• Spartan-6 LXT	Xilinx SP605 Development Kit
• Kintex-7	Xilinx KC705 Evaluation Kit
• Virtex-4 FX	Xilinx ML405 Development Kit
• Virtex-5 LXT	Xilinx ML555 Development Kit
• Virtex-5 FXT	Xilinx ML507 Development Kit
• Virtex-6 LXT	Xilinx ML605 Development Kit
• Virtex-7	Xilinx VC707 Evaluation Kit
• Kintex-UltraScale	BETA (full working TB and example)

All deliveries include VHDL and Verilog simulation models, a self-checking testbench with simulation scripts, and ready-to-run design targeted at a popular development board for each family (listed above).